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The ARM processor family

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General Introduction of ARM (1)

- Advanced Reduced-instruction-set-computer Machine:
  - typical RISC features:
    - large uniform register file
    - load/store architecture
    - simple addressing modes
    - uniform and fixed-length instruction fields
  - enhancements to a basic RISC architecture:
    - control over ALU and shifter in most data-processing instructions
    - auto-increment and auto-decrement addressing modes
    - load and store multiple instructions
    - conditional execution of almost all instructions

General Introduction of ARM (2)

- ARM registers:
  - 31 general-purpose 32-bit registers:
    - 16 of these visible, the other are used to speed up exception processing
    - three of the 16 visible registers have special roles:
      - stack pointer: normally used R13
      - link register: normally used R14
      - program counter: normally used R15
  - 6 32-bit status registers (one for each exception mode):
    - Current program status register (CPSR): it mainly holds
      - four condition code flags (Negative, Zero, Carry and oVerflow)
      - flags for overflow conditions (Q and GE flags)
      - two interrupt disable bits, one for each type of interrupt
      - type of instruction set / processor mode
      - Saved program status register (SPSR)

General Introduction of ARM (3)

- ARM instruction sets:
  - ARM instruction set:
    - branch instruction
    - data-processing instructions
    - status register transfer instructions
    - load and store instructions
    - coprocessor instructions
    - exception-generating instructions
  - Thumb instruction set: subset of ARM instruction set in which each instruction is encoded in 16 bits instead of 32 bits

General Introduction of ARM (4)

- ARM programmers' model:
  - data types:
    - byte
    - halfword
    - word
  - processor modes:
    - User: normal program execution mode
    - FIQ: high-speed data transfer or channel process
    - IRQ: general-purpose interrupt handling
    - Supervisor: protected mode for the operating system
    - Abort: implements virtual memory and/or memory protection
    - Undefined: supports software emulation of hardware coprocessors
    - System: runs privileged operating system tasks

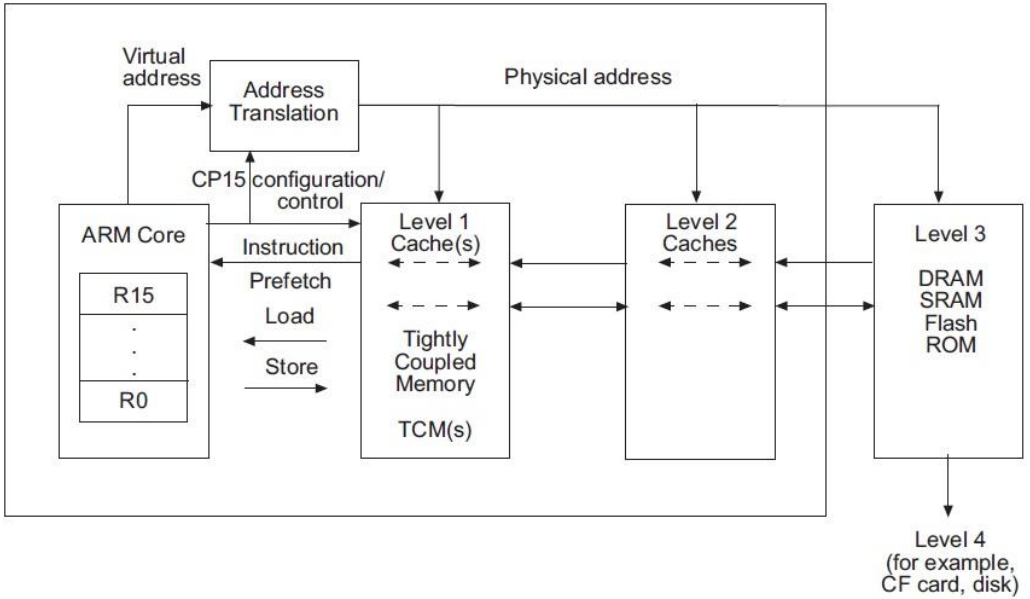
General Introduction of ARM (5)

- ARM exceptions:
  - they are generated by internal and external sources to cause the processor to handle an event
  - processor state before handling the exception is preserved
  - more than one exception can arise at the same time.
  - seven types of exception:
    - different priorities
    - managed through processor modes

Priority		Exception
Highest	1	Reset
	2	Data Abort (including data TLB miss)
	3	FIQ
	4	IRQ
	5	Imprecise Abort (external abort) - ARMv6
	6	Prefetch Abort (including prefetch TLB miss)
Lowest	7	Undefined instruction SWI

General Introduction of ARM (6)

- ARM Memory architecture (1):
  - memory hierarchy dependent on overall system performance & costs goals
  - to point out the main features consider the following example:



General Introduction of ARM (7)

- ARM Memory architecture (2):
  - Caches:
    - size and organization readable from CP15’s read-only Register 0
  - Tightly Coupled Memory (TCM): provide low latency memory that can be used by the processor without the unpredictability that is a feature of caches
  - System Control coprocessor (CP15): it manages standard memory and system facilities
  - Virtual Memory System Architecture (VMSA): control virtual-to-physical address mapping, access permissions to memory, and other memory attributes, based on the use of a Memory Management Unit (MMU)

Set of ARM processors

Widest range of microprocessor cores to address the performance, power and cost requirements for almost all application markets.

Cortex-A

Cortex-R

Cortex-M

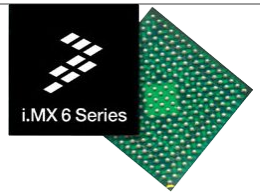
SecurCore

Processors grouped as follows:

- Cortex - A: Highest performance, optimized for rich operating systems
- Cortex - R: Fast response, optimized for high-performance, hard real-time applications
- Cortex - M: Smallest/lowest power, optimized for discrete processing and microcontroller
- SecurCore: Tamper resistant, optimized for security applications

Embedded vs Application processor

- ARM M processors and ARM A processors

 ARM M core	 ARM A core
Single Core	Multi Core capable
< 550MHz	< 2.5Ghz
Single Application targeted	Operating System targeted
Low Power focused	High computational Power focused

Embedded vs Application processor

- Major Core differences

ARM A:

Support Features which are negligible for ARM M processors such as:

MMU & MPU

External Memory interface

ARM M:

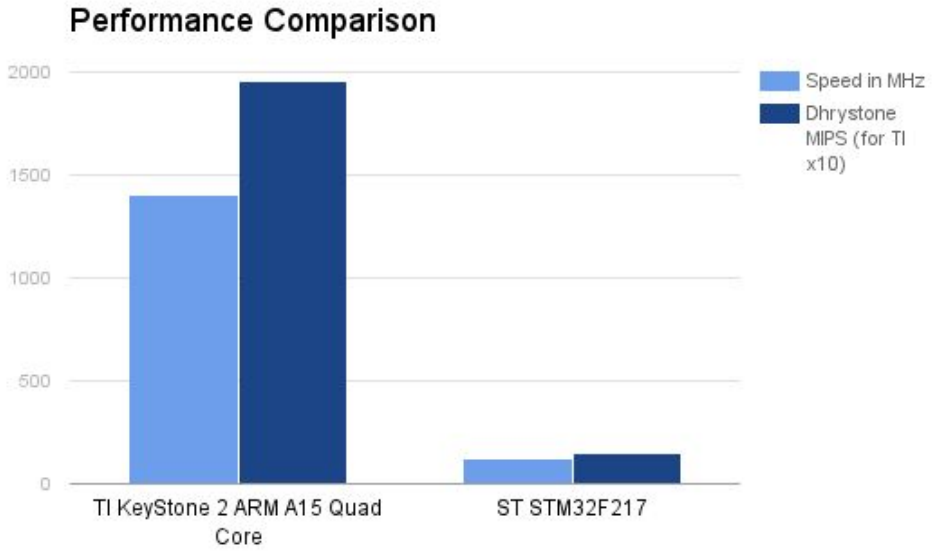
Have more advanced Features in terms of low power operation such as:

Several low power operating mods

Power consumption optimized peripherals

Embedded vs Application processor

- Performance difference



Embedded vs Application processor

- Applications

ARM M:

IoT Products
Wearables
Real Time Control
Co- Processing

ARM A:

Multimedia Appliances
Car Infotainment
Smartphones
Demanding computational Tasks

ARM 11 (ARMv6 architecture)

- Raspberry PI V1

The Raspberry Pi is a credit card-sized single-board computers developed to promote the teaching of basic computer science in schools and in developing countries. Developed by the Raspberry Pi Foundation in the United Kingdom.

ARM 11 (ARMv6 architecture)

- Main Features
  - Broadcom BCM2835 SOC
  - 700MHz ARM1176JZF-S (ARM11) processor (ARM v6 architecture)
  - Performance equal to an 300MHz Pentium2
  - L1/L2 Cache 16KB/128KB
  - 512MB RAM
  - integrated GPU
- Commercial Products
  - Slice Media Player
  - OTTO GIF Camera

Example of embedded ARM processor: Cortex-M3

- Offers superior efficiency and flexibility and is specifically developed for response and power sensitive applications
- Thumb-2 Instruction Set Architecture (ISA)
  - supports 16- and 32-bit instructions
  - can be mixed without extra complexity and without reducing the Cortex-M3 performance
- 3-stage Pipeline Core Based on Harvard Architecture
  - reduced bottlenecks common to shared data and instruction buses
- Quickly Servicing Critical Tasks and Interrupts
  - from the low energy modes, it is active within 2 µs and delivers 1.25 DMIPS/MHz
  - up to 240 physical interrupts with 1-256 levels of priority
- Reducing the 32-bit Footprint
  - small footprint reduces system cost
  - reduced application's active periods (the periods where the CPU is handling data) increases the application's battery lifetime significantly

Bibliography

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- Silicon Labs official website: https://www.silabs.com
- TI KeyStone II: https://training.ti.com/system/files/docs/keystone-ii-arm-a15-corepac-overview.pdf